AMENDMENTS TO THE DRAWINGS:

Subject to the approval of the Examiner, Applicants propose to amend Figures 1-11, 12A, 12B, 12C, 13, and 14 as indicated on the annotated drawing replacement sheet labeled Replacement Sheets 1/13 through 13/13 attached hereto.

Attachments:

Replacement Sheets 1/13 through 13/13, including Figures 1-11, 12A, 12B, 12C, 13, and 14

Annotated Sheet showing changes to Figures 1-11, 12A, 12B, 12C, 13, and 14

REMARKS

In the Office Action mailed April 17, 2006,[1] the Examiner objected to the specification because the title is allegedly not descriptive; objected to the drawings; rejected claim 41 under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter; rejected claims 6, 20, and 34 under 35 U.S.C.§ 112, second paragraph; and rejected claims 1-41 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,633,856 to Richardson et al. ("*Richardson*").

Applicants have amended the title and specification; amended Figures 1-11, 12A, 12B, 12C, 13, and 14; and amended claims 1, 2, 6, 7, 8, 14, 15, 18, 20, 21, 27, 28, 31, 32, 34, 40, and 41. Claims 1-41 remain pending.

Though Applicants disagree with the Examiner's objection to the title, Applicants have amended the title to read: "Decoding Apparatus, Decoding Method, and Program to Decode Low Density Parity Check Codes." Applicants have also amended the specification to correct a typographical error.

Applicants respectfully request reconsideration and withdrawal of the objection to the drawings. The drawings comply with 37 C.F.R. § 1.83(a) because Applicants have amended Figures 1-11, 12A, 12B, 12C, 13, and 14 as suggested by the Examiner on page 2 of the outstanding Office Action. Specifically, Applicants have amended Figures 1-11, 12A, 12B, 12C, 13, and 14 to include the label "Prior Art."

Applicants respectfully traverse the rejection of claim 41 under 35 U.S.C. § 101, as allegedly directed to non-statutory subject matter. To advance prosecution,

---

[1] The Office Action may contain statements characterizing the related art, case law, and claims. Regardless of whether any such statements are specifically identified herein, Applicants decline to automatically subscribe to any statements in the Office Action.

however, Applicants have amended claim 41 to recite in-part "[a] computer readable medium having a program for causing a computer to perform a decoding method for use with a decoding apparatus for decoding Low Density Parity Check ("LDPC") codes...." Thus, because claim 41 is directed toward statutory subject matter, Applicants respectfully request the Examiner withdraw the rejection of claim 41 under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Applicants respectfully traverse the rejection of claims 6, 20, and 34 under 35 U.S.C.§ 112, second paragraph.

With respect to claim 6, the Examiner alleges that claim 6 should read: "...when the sub-matrices whose weight is 2 or more from among the sub matrices representing said check matrix are represented in the form of the sum of the unit matrix, ~~**whose weight is 1**~~, the quasi-unit matrix, or the shift matrix **whose weight is 1**." (Office Action at 3.) Applicants respectfully disagree. Applicants specification, for example, states in-part, "for the sub-matrix whose weight is 2 or more, the data (the message corresponding to the edges belonging to the unit matrix, the sum matrix, or the shift matrix) corresponding to the positions of 1s of the unit matrix whose weight is 1, the quasi-unit matrix, or the shift matrix, when the sub-matrix is represented in the form of the sum of two or more of the (P x P) unit matrix whose weight is 1...." (*Specification*, p. 52, lines 18-25.) (emphasis added.) Thus, based at least on the above-referenced portions of Applicants' specification, claim 6 particularly points out and distinctly claims that the weight of one corresponds to the unit matrix's weight, rather than to the shift matrix as alleged by the Examiner. Applicants therefore request that the Examiner withdraw the rejection of claim 6 under 35 U.S.C.§ 112, second paragraph.

With respect to the rejection of claims 20 and 34 under 35 U.S.C.§ 112, second paragraph, the Examiner alleges that claims 20 and 34 should read: "[t]he decoding apparatus according to claim 18, wherein said first decoding in-progress results stored at the same address in each of said two single-port RAMs." (Office Action at 3.) Amended claims 20 and 34 recite in-part, "said two single-port RAMs each read said second decoding in-progress results stored at the same address, where said decoding in-progress results were previously stored." Applicants specification discloses, for example, "the RAM 503...reads...the decoding in-progress results D502 corresponding to 1s from the sixth row to the 10th row, which are stored at the same address, from among the decoding in-progress results D502 obtained as a result of the first computation...at the previous time, which are already stored." (*Specification*, p. 108, lines 8-15; *see also* p. 107, lines 18-25.) In view of the foregoing, Applicants request withdrawal of the rejection of claims 20 and 34 under 35 U.S.C.§ 112, second paragraph.

Applicants respectfully traverse the rejection of claims 1-41 under 35 U.S.C. § 102(b) as being anticipated by *Richardson*. To properly establish that a prior art reference anticipates a claimed invention under 35 U.S.C. § 102, each and every element of the claims in issue must be found, either expressly described or under principles of inherency, in the single prior art reference.

Applicants submit that independent claim 1 is not anticipated by *Richardson* because the reference fails to teach each and every claim element of the claim. In particular, *Richardson* at least fails to disclose a decoding apparatus including, for example, "first computation means for simultaneously performing P check node

computations" and "second computation means for simultaneously performing P variable node computations," as recited in independent claim 1.

Richardson discloses that "[s]ince the decoding techniques of the present invention allow for a large number of decoding operations...to be performed in parallel, the decoders of the present invention can be used to decode received words at high speeds." *Richardson*, col. 11, lines 12-17. *Richardson* also discloses "performing both variable node and constraint node processing operations...at the same, e.g., simultaneously and independently." *Richardson*, col. 24, lines 37-41 (emphasis added). Performing both variable node and constraint node processing operations "simultaneously," as disclosed by *Richardson*, merely means that the variable and constraint node vector processors perform their respective processing operations at the same time as each other. Such teachings, however, do not indicate that either of the processors, individually, performs P number of node vector computations simultaneously, let alone either "simultaneously performing P check node computations" or "simultaneously performing P variable node computations." *Richardson*, therefore, fails to teach or suggest a decoding apparatus including, for example, "first computation means for simultaneously performing P check node computations" and "second computation means for simultaneously performing P variable node computations," as recited in independent claim 1.

In view of the foregoing, Applicants submit that independent claim 1 is allowable over *Richardson*. Accordingly, Applicants request reconsideration and withdrawal of the rejection based on *Richardson*. Independent method claim 40 and independent computer media claim 41, while of different scope than independent apparatus claim 1,

recite subject matter similar to that of independent claim 1 already discussed. Independent claims 40 and 41, therefore, are allowable at least for the reasons presented above for independent claim 1.

In addition, claims 2-39 are allowable at least because of their dependence from allowable independent claim 1, as well as because of the recitations of those claims.

For example, claim 14 is not anticipated by *Richardson* because the reference does not disclose a decoding apparatus where, for example, "said first computation means performs some of said P check node computations and said P variable node computations" and "said second computation means performs some of the others of said P variable node computations," as recited in claim 14.

In rejecting claim 1 under 35 U.S.C. § 102(b), the Examiner alleges that the constraint node vector processor 1609 of *Richardson* is the claimed "first computation means" and the variable node vector processor 1608 is the claimed "second computation means." (Office Action at 4-5.) Assuming that the Examiner's allegations are correct (and Applicants do not agree that they are) according to *Richardson*, the constraint node vector processor 1609 only performs constraint mode processing operations and the variable node vector processor 1608 only performs variable node processing operations. *Richardson*, col. 24, lines 48-55.

Richardson, if anything, discloses that constraint node vector processing and variable node vector processing may be performed simultaneously. *Richardson*, col. 24, lines 38-41. Providing two separate components that may performing constraint node and variable node vector processing simultaneously does not indicate that either the constraint node vector processor or the variable node processor perform both

constraint node and variable node vector processing, respectively. Moreover, in *Richardson*, it appears that respective processors perform all of their respective node vector processing, as opposed to some of their respective node vector processing. *Richardson*, col. 24, lines 31-67; col. 25, lines 1-38; *see also* Figure 16. Thus, because neither of the node vector processors in *Richardson* perform both constraint node and variable node vector processing, and because the node vector processors perform all of their respective node vector processing, *Richardson* fails to teach or suggest a decoding apparatus where, for example, "said first computation means performs some of said P check node computations and said P variable node computations" and "said second computation means performs some of the others of said P variable node computations," as recited in claim 14.

In view of the arguments presented above, *Richardson* does not teach each and every element of claim 14, and thus, does not anticipate claim 14. In addition to being allowable based on their dependence from independent claim 1, claims 15-39 are allowable based on their dependence from claim 14.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 17, 2006

By: _____
Patrick L. Miller
Reg. No. 57,502

Attachments:

Replacement Sheets 1/13 through 13/13, which include Figures 1-11, 12A, 12B, 12C, 13, and 14 (13 pages)

Annotated Sheets showing changes to Figure 1-11, 12A, 12B, 12C, 13, and 14 (13 pages)

FIG. 1 - Prior Art

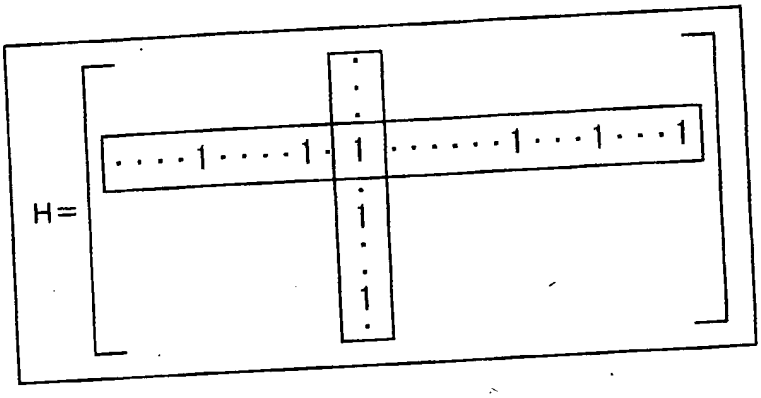


FIG. 2 - Prior Art

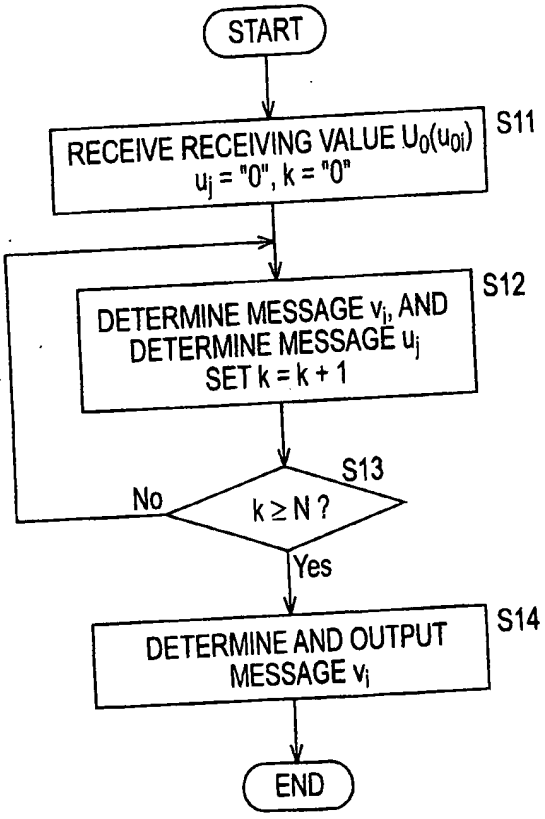


FIG. 3 - Prior Art

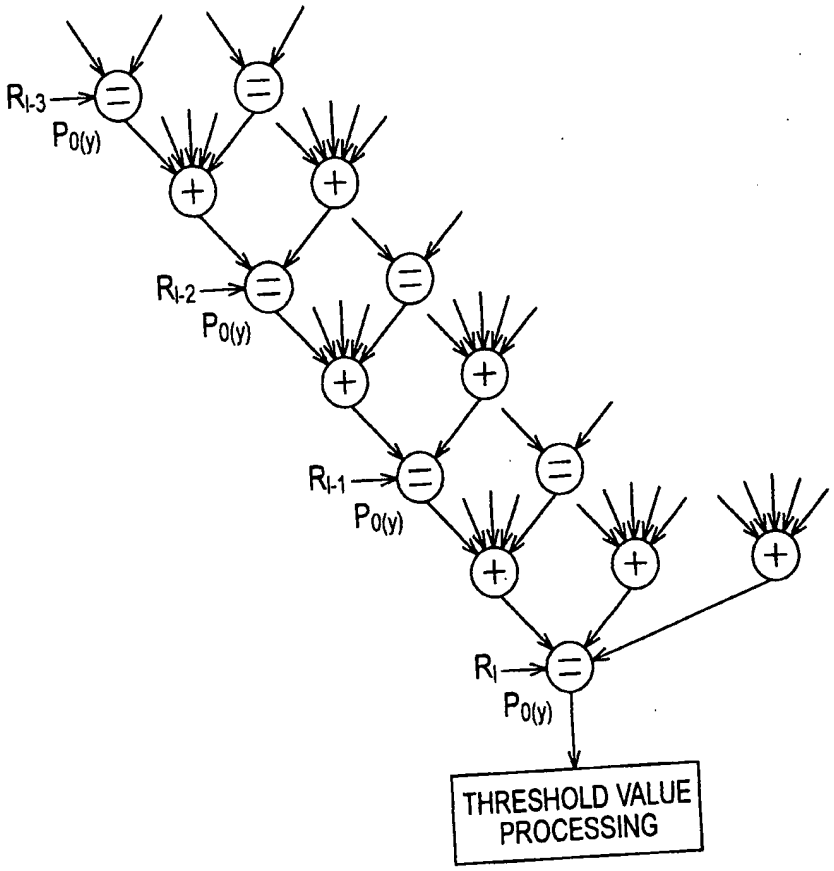


FIG. 4 - Prior Art

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

FIG. 5 - Prior Art

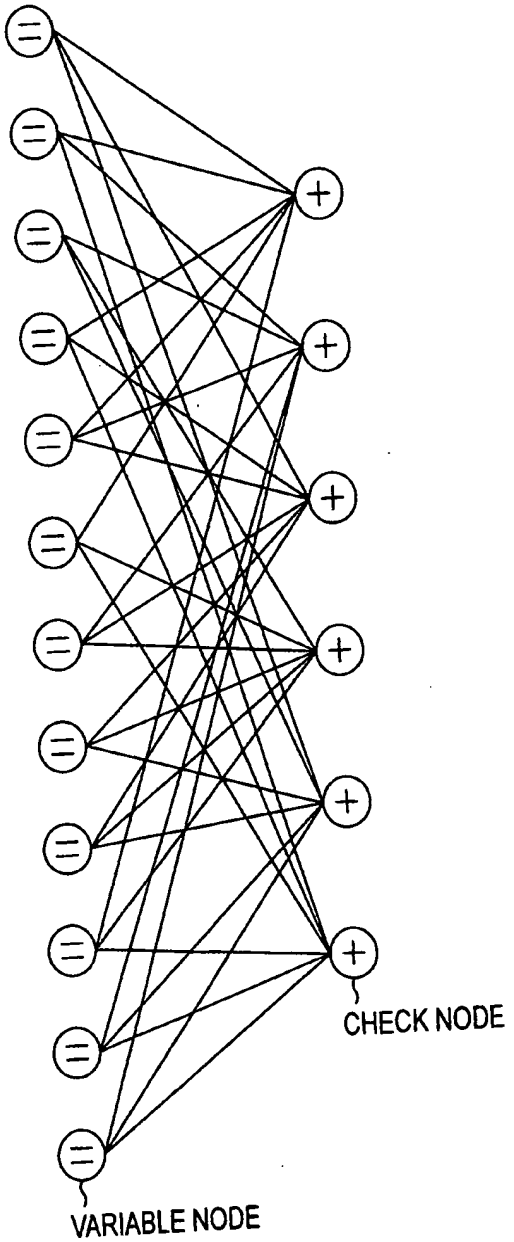


FIG. 6 - Prior Art

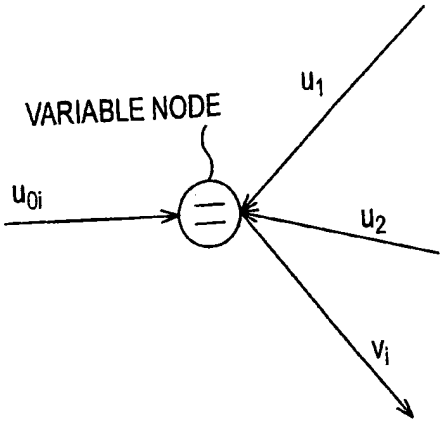
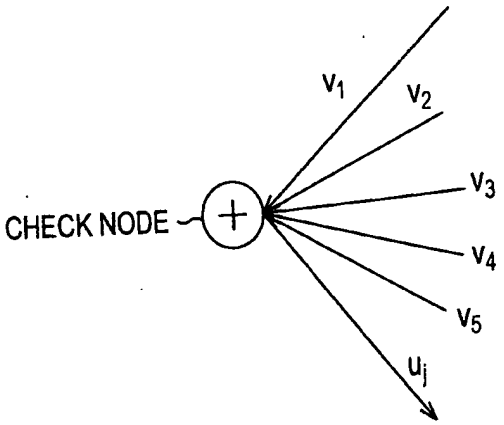


FIG. 7 - Prior Art



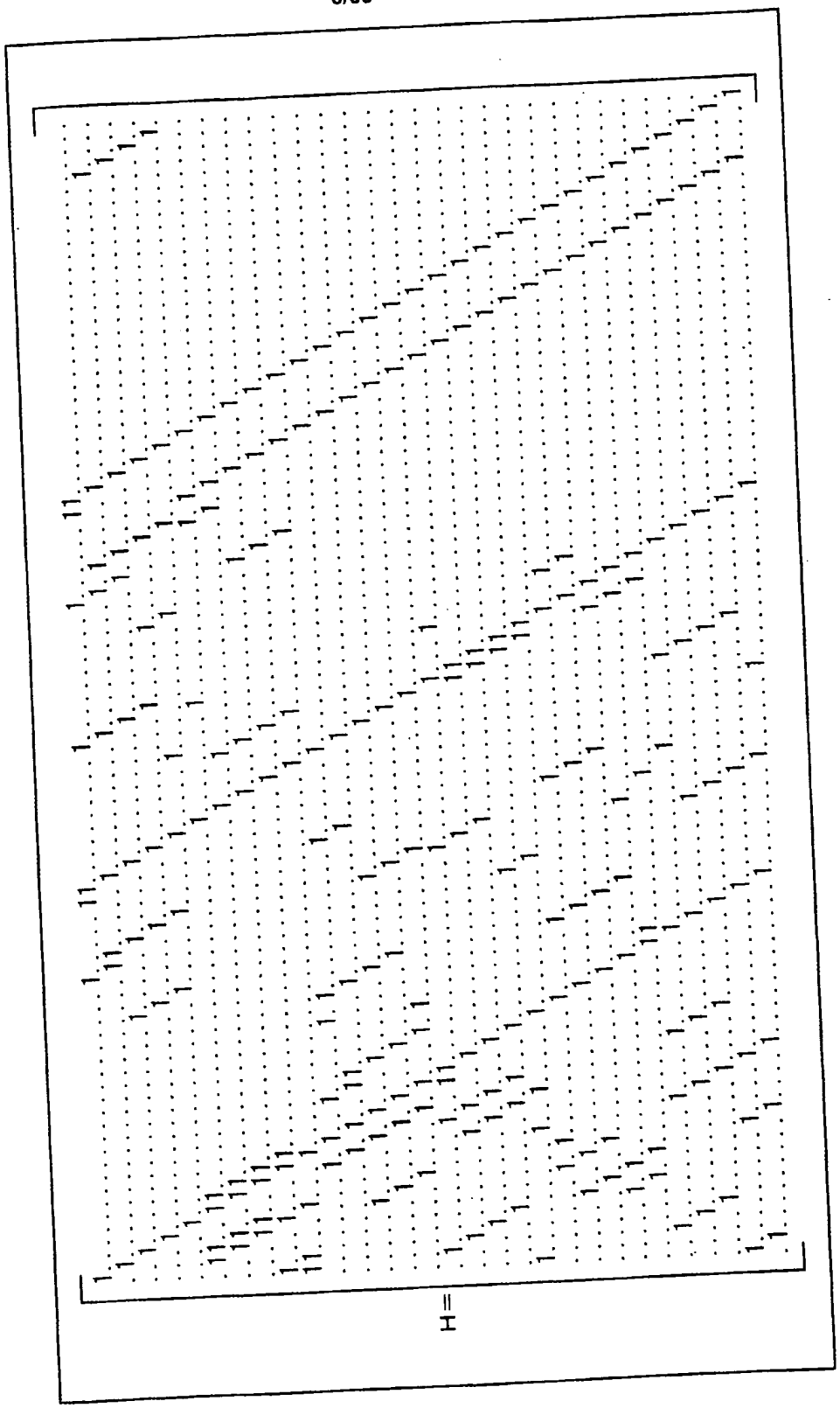
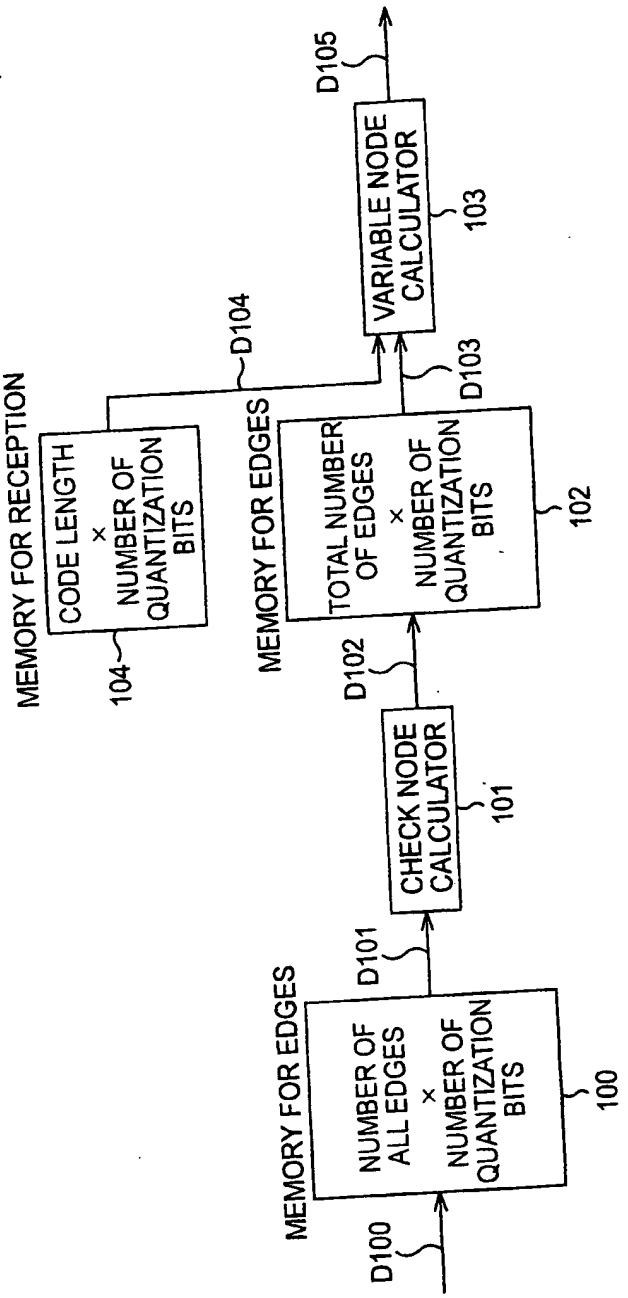


FIG. 8 - Prior Art

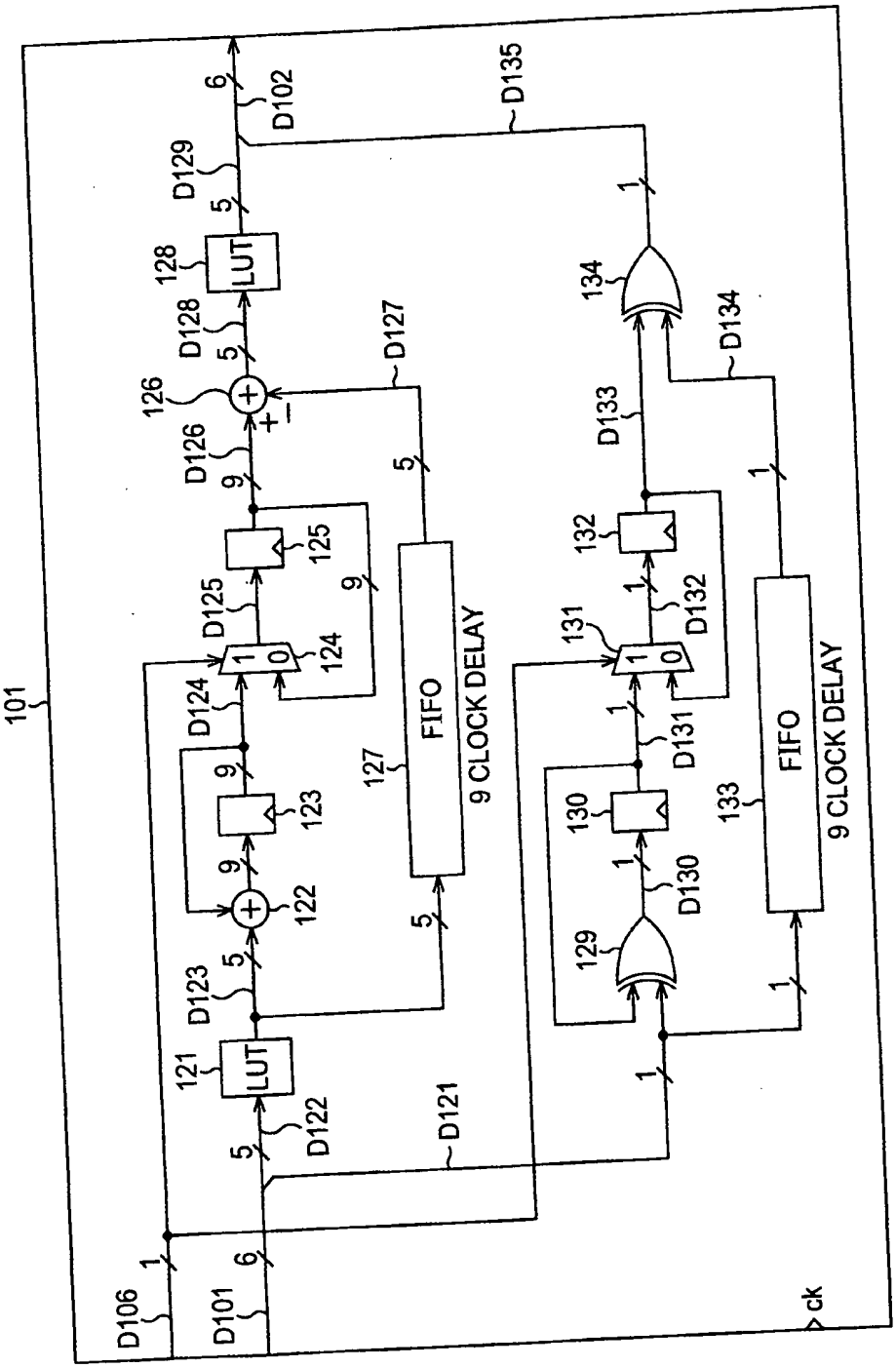
Replacement Sheet 6/13

FIG. 9 - Prior Art



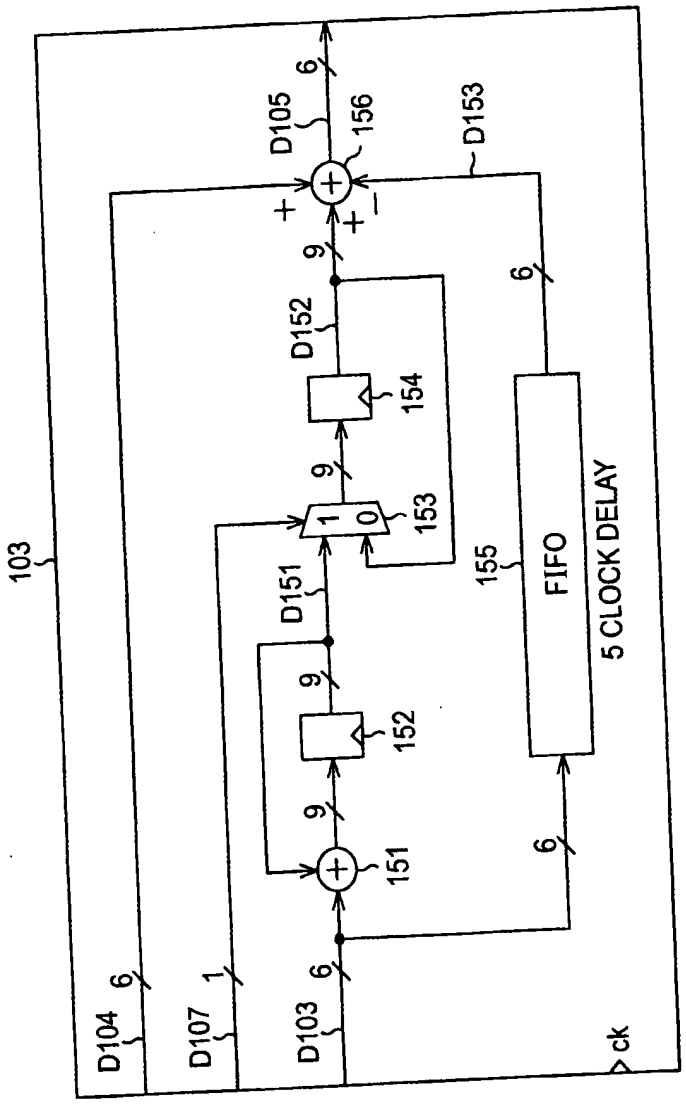
Replacement Sheet 7/13

FIG. 10 - Prior Art



Replacement Sheet 8/13

FIG. 11 - Prior Art



Replacement Sheet 9/13

FIG. 12A - Prior Art

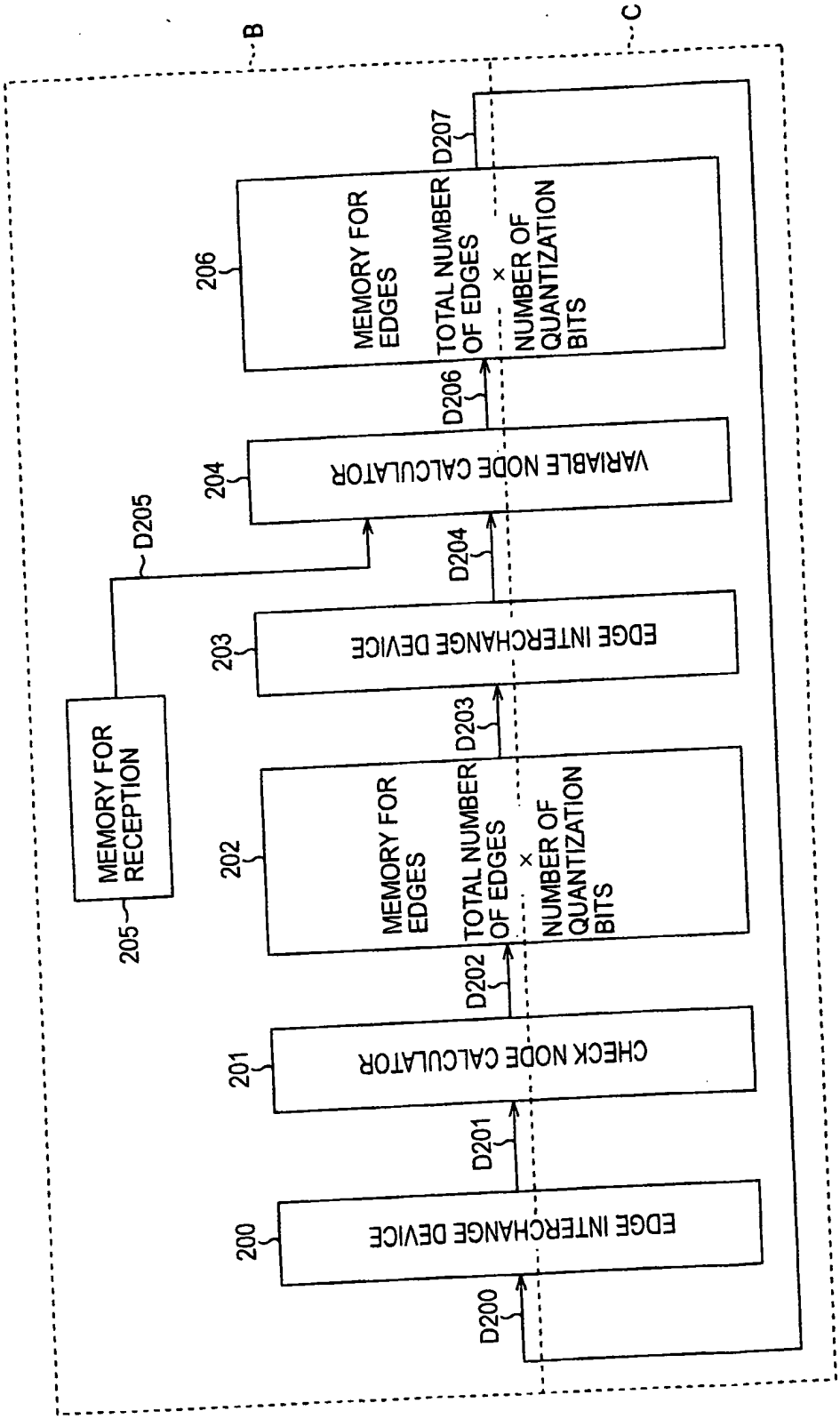
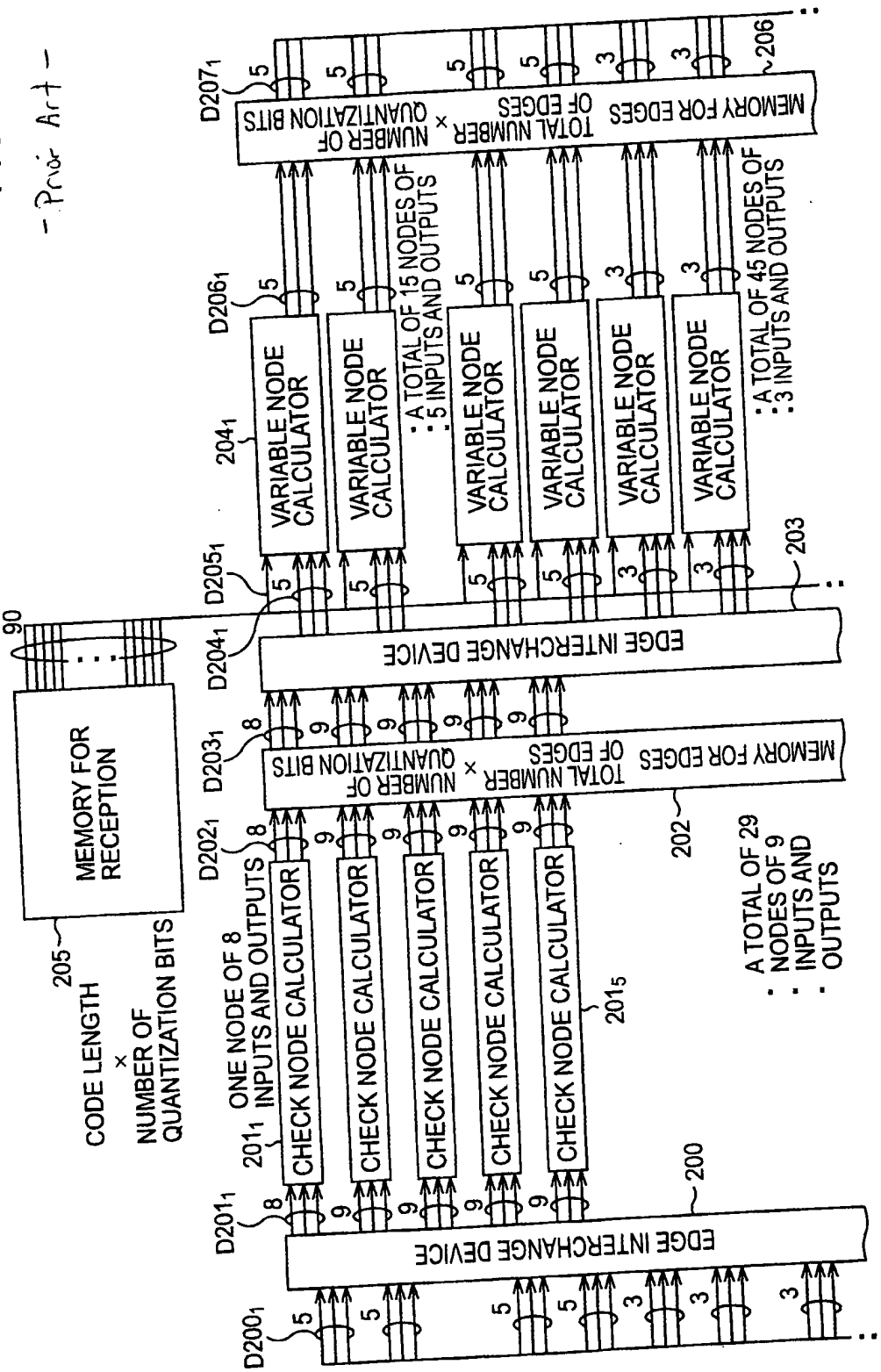


FIG. 12B

- Prior Art -



Replacement Sheet 11/13

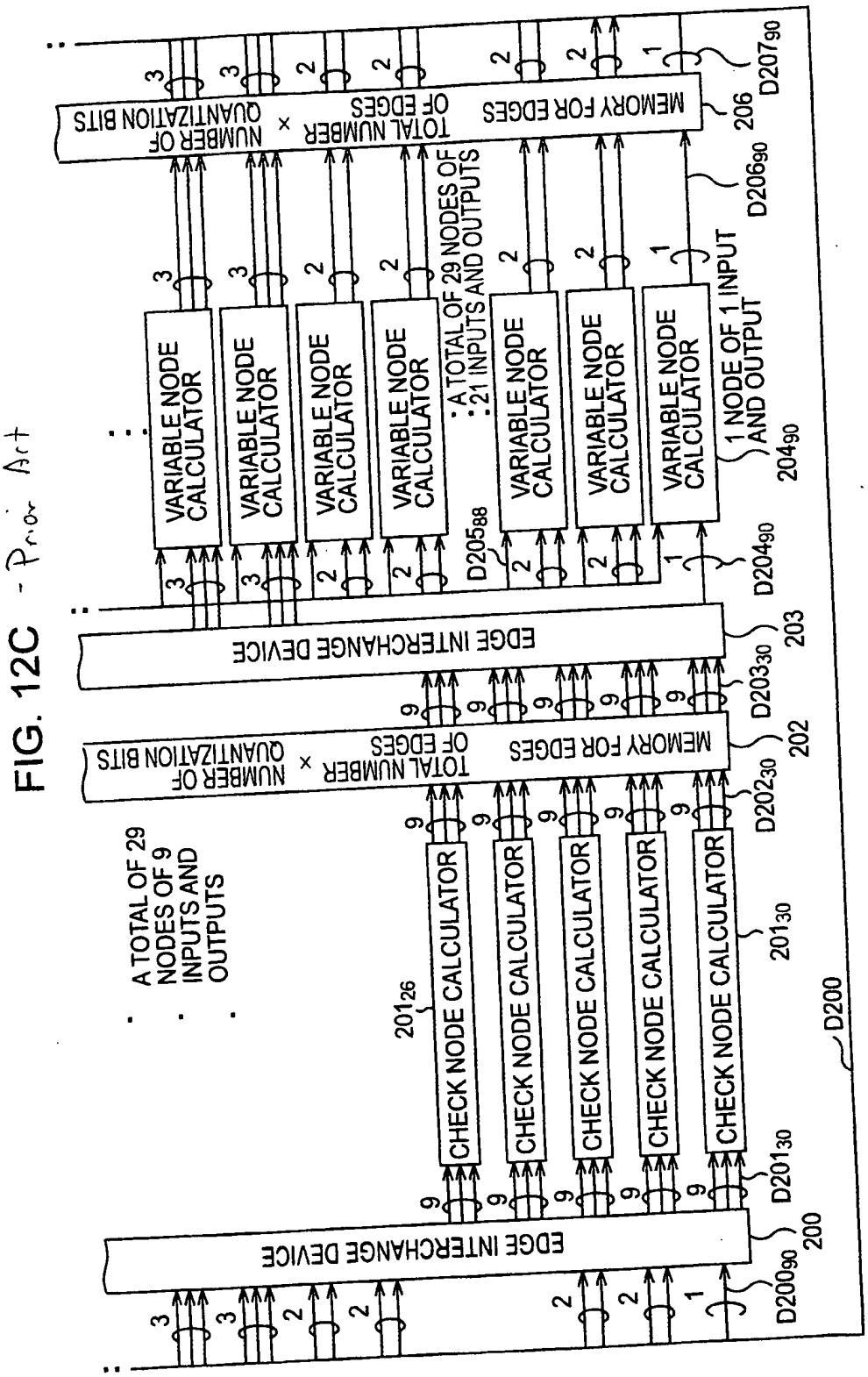


FIG. 12C - Prior Art

FIG. 13 - Prior Art

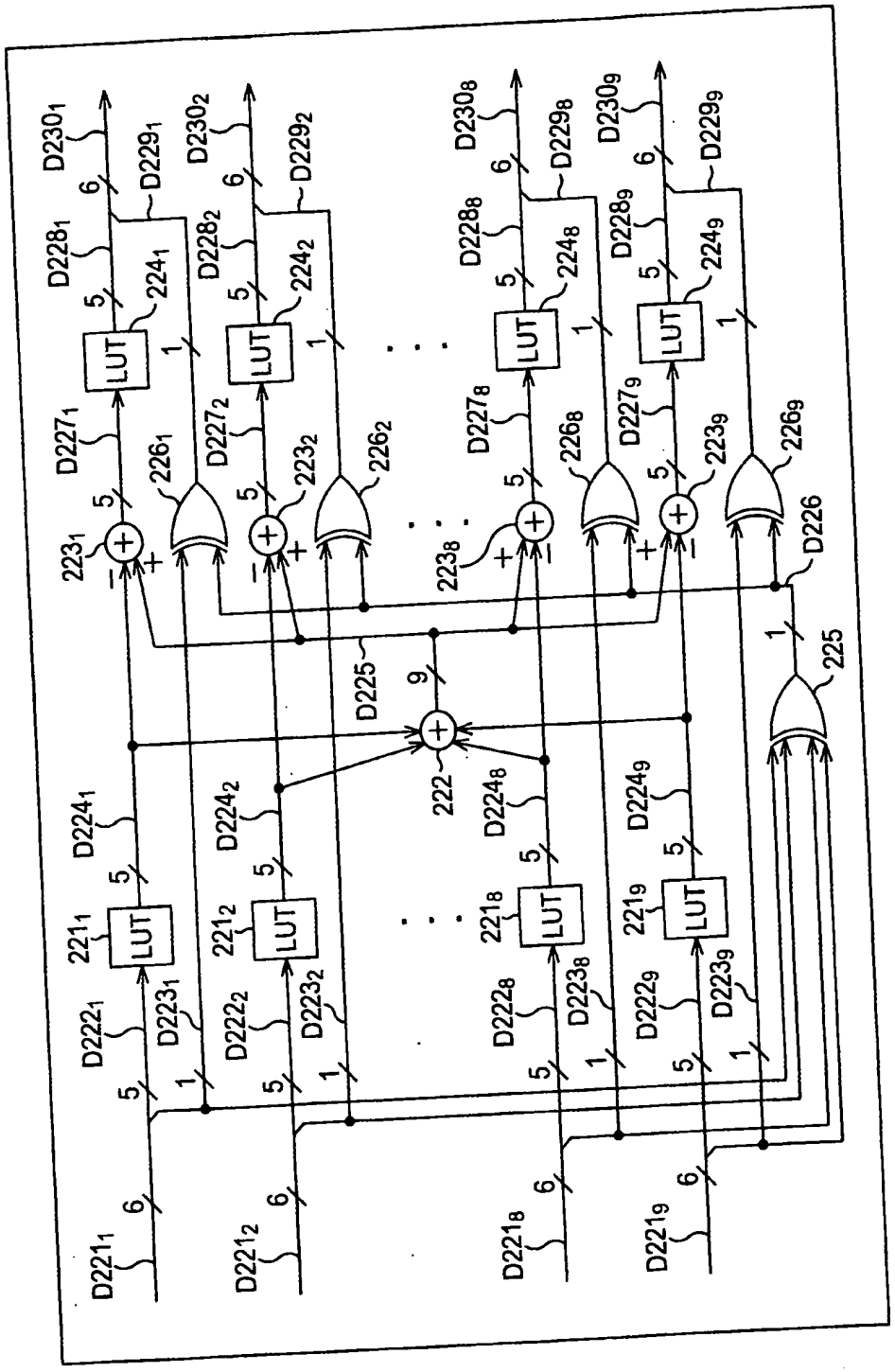


FIG. 14 - Prior Art